



### REMARKS/ARGUMENTS

Claim 1 is unchanged. Claims 2-17 have been added.

It is noted that the specification filed in this case is in the form of the substitute specification that was filed on February 18, 2004 in the parent application (No. 10/262,567). That substitute specification was accepted by the Examiner in the parent case.

The amendments to the specification made herein are intended to conform the specification to the amendments in the drawings, described in the preceding section, and to correct several remaining clerical and syntactical errors. No new matter has been added.

A complete set of formal drawings is submitted herewith.

Should the Examiner have any questions about any of the amendments made herein, the Examiner is invited to call the undersigned at (408) 982-8201.

#### **CERTIFICATE OF MAILING BY "FIRST CLASS"**

I hereby certify that this paper or fee is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the below date.

Attorney for Applicant(s)

8/8/05

Date of Signature

Respectfully submitted,

David E. Steuber  
Attorney for Applicant(s)  
Reg. No. 25,557

**Amendments to the Drawings:**

The enclosed Submission of Formal Drawings includes changes to Figs. 14A-14E, 14H-14P, 15A, 16A, 16B, 16D, 16F, 17P-17CC (now Figs. 17O-17BB), 18B (now Fig. 18B-4), 18C, 18H, 19H, 33D and 64B.

The following is an itemization of the changes:

In Figs. 14A-14E, 14H-14P, 15A, 16A, 16B, 16D and 16F, in a number of instances the reference numeral PW5 has been changed to PW5B, the reference numeral NW5 has been changed to NW5B, the reference numeral PW12 has been changed to PW12B, and the reference numeral NW12 has been changed to NW12B, as shown on the enclosed Annotated Sheets. These changes are clearly supported, for example, at page 36, lines 14-17, of the substitute specification filed February 18, 2004, where it is indicated that the suffix "B" is used to denote an implanted layer of dopant as opposed to a "well" of dopant. In any event, these changes are merely changes in labeling and as such do not constitute new matter.

Figs. 17P-17CC have been renumbered as Figs. 17O-17BB, respectively, to rectify the omission of Fig. 17O from the application as filed.

To make the drawings more legible, Figs. 18A and 18B have each been split into four drawings, designated Figs. 18A-1 to 18A-4 and Figs. 18B-1 to 18B-4, respectively. The subject matter in Figs. 18A-1 to 18A-4 and 18B-1 to 18B-3 is unchanged. In Fig. 18B-4, the reference numeral 354M has been replaced by the numeral 354L. The numeral 354M was an error. There is no such reference numeral in the application as filed.

In Fig. 18C, the reference numeral 364P, which is referred to at page 66, line 4, of the substitute specification, has been added, and the designation of the source-body contact has been corrected from "S/D" to "S/B".

In Fig. 18H, reference numeral applicable to the well NW5 has been changed from 354R to 354S to eliminate the conflict with the similarly numbered element in Fig. 18G; and

the reference numeral applicable to the deep N layer has been changed from 390G to 390H to eliminate the conflict with the similarly numbered element in Fig. 35A.

In Fig. 19H, the reference numeral 387 has been corrected to 320 to correspond to the designation of the DMOS transistor at page 70, line 7, of the substitute specification.

In Fig. 33D, the reference numeral 486 has been deleted. It is not referenced in the substitute specification.

In Fig. 64B, the description of the 5 volt transistor 306 as been corrected to "PNP."

All of the foregoing changes are shown in red in the enclosed Annotated Marked-up Drawings.

Finally, to place the drawings in sequential order, sheets 215-218 (Figs. 17V-17CC) of have been renumbered as sheets 75-78 (renumbered Figs. 17U-17BB), and sheet 219 (Fig. 18H) has been renumbered as sheet 92.

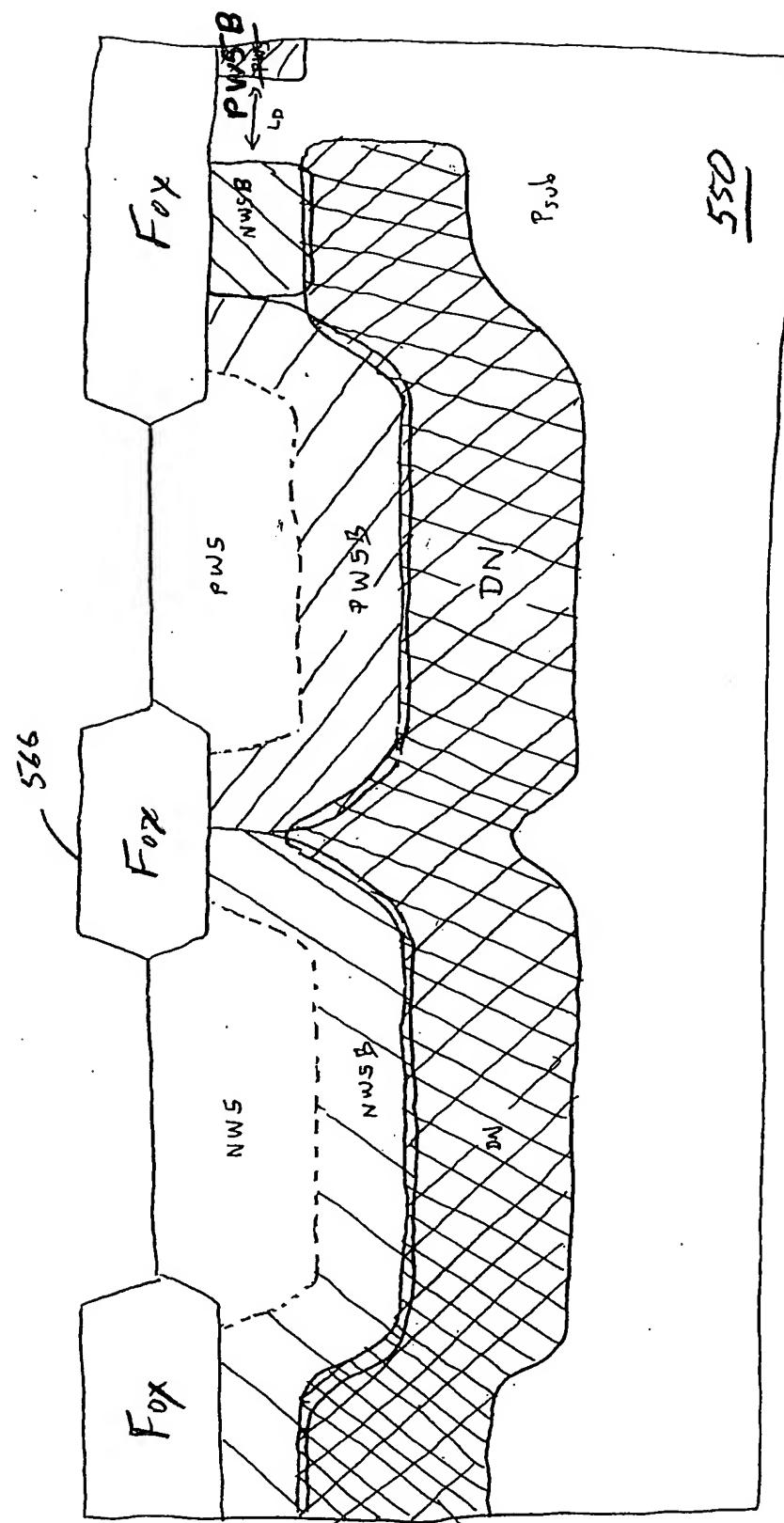
All of the foregoing amendments are incorporated in the Submission of Formal Drawings, enclosed herewith.

Attachment: Annotated Sheets Showing Changes



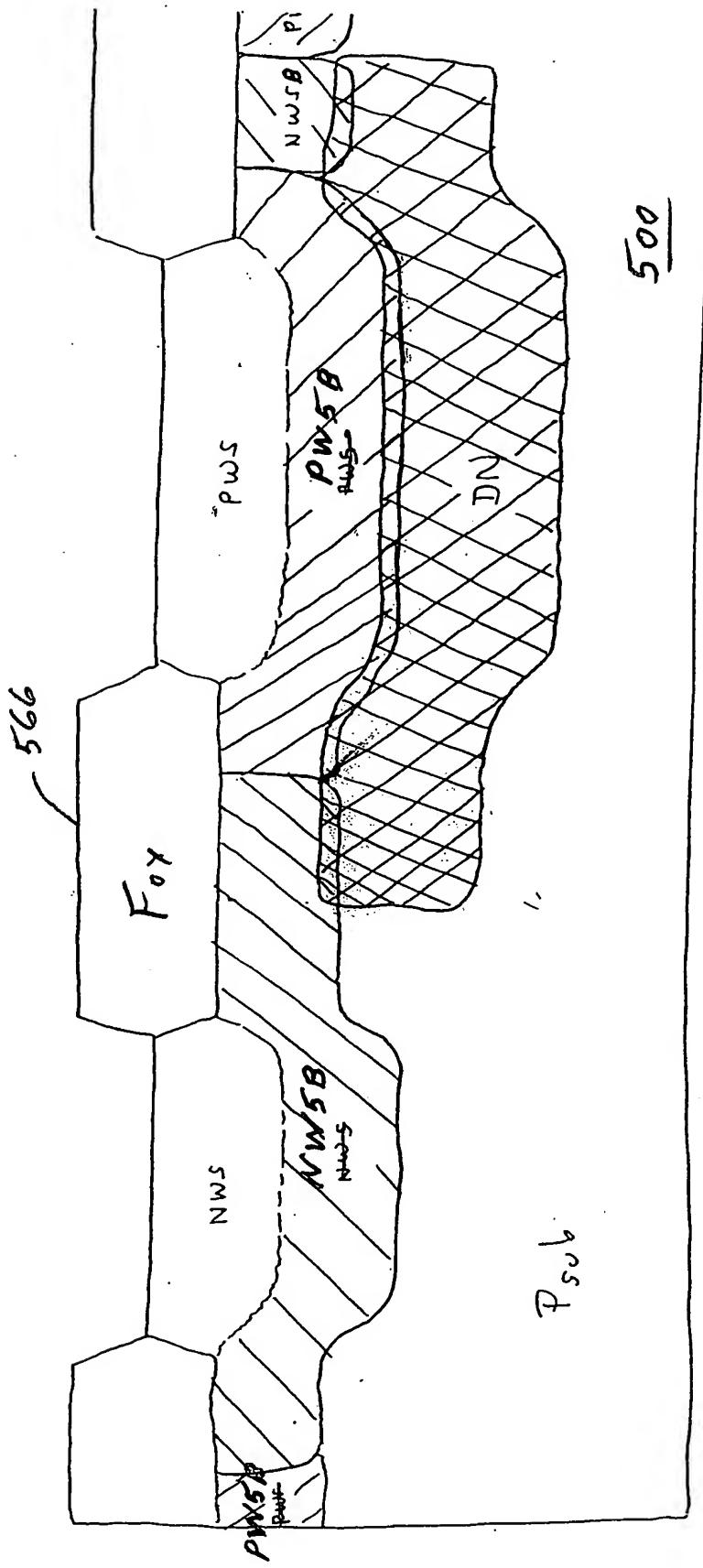
43/219

Fig 14A



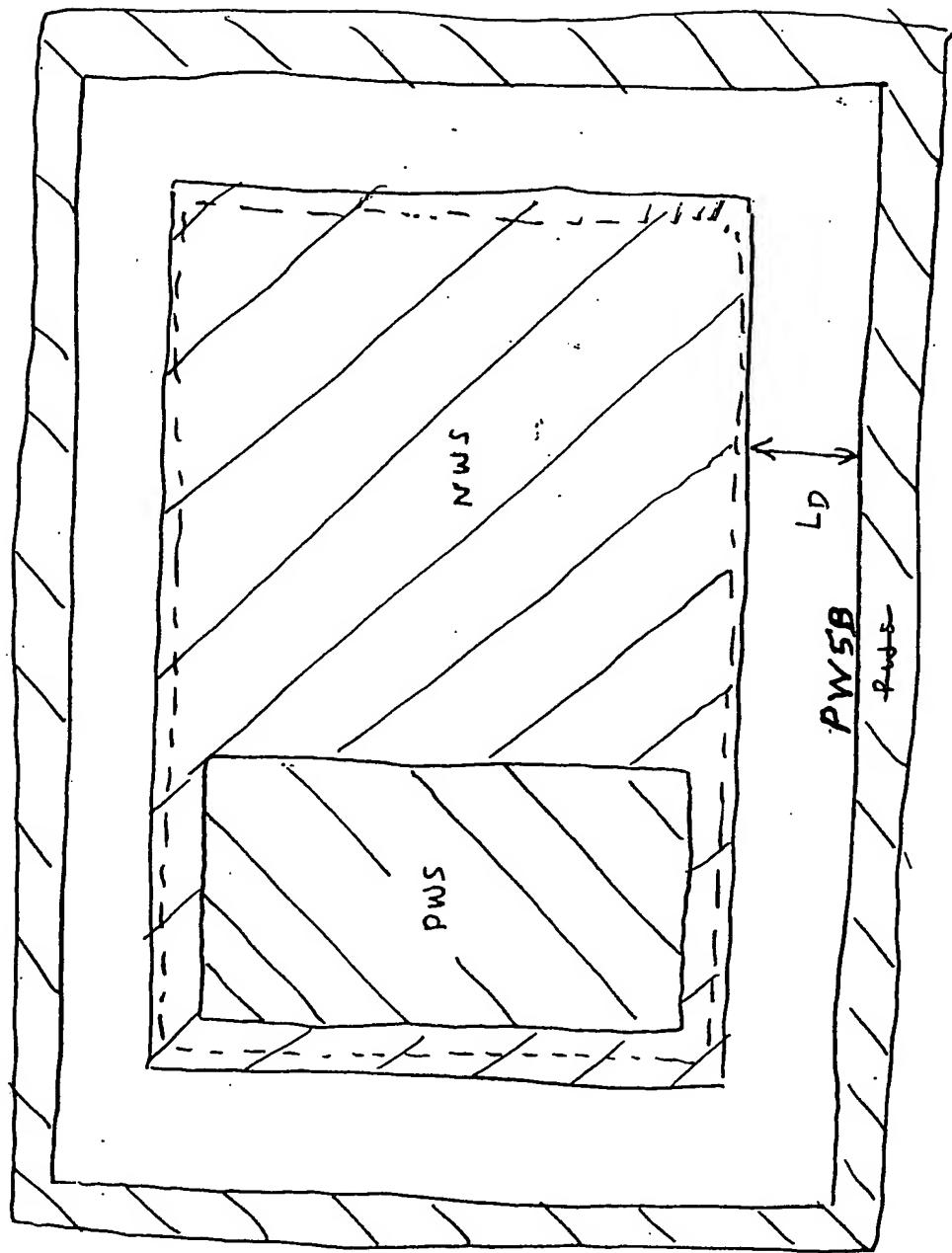
44/219

Fig. 14 B.



45/219

Fig. 141 C



46/219

Fig. 14 E

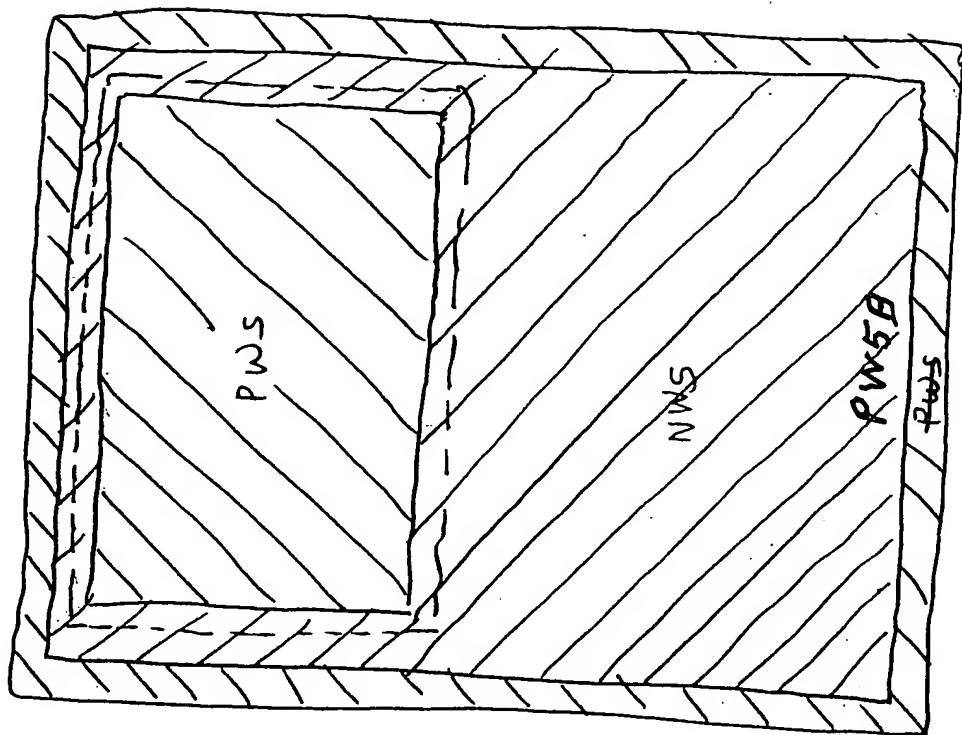


Fig. 14 D

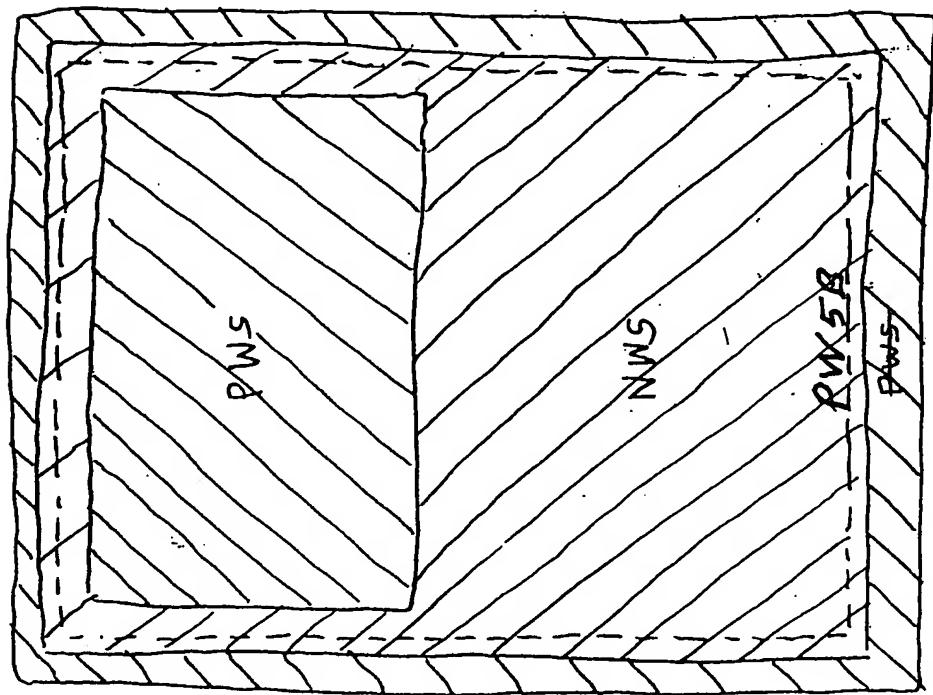


Fig. 14H

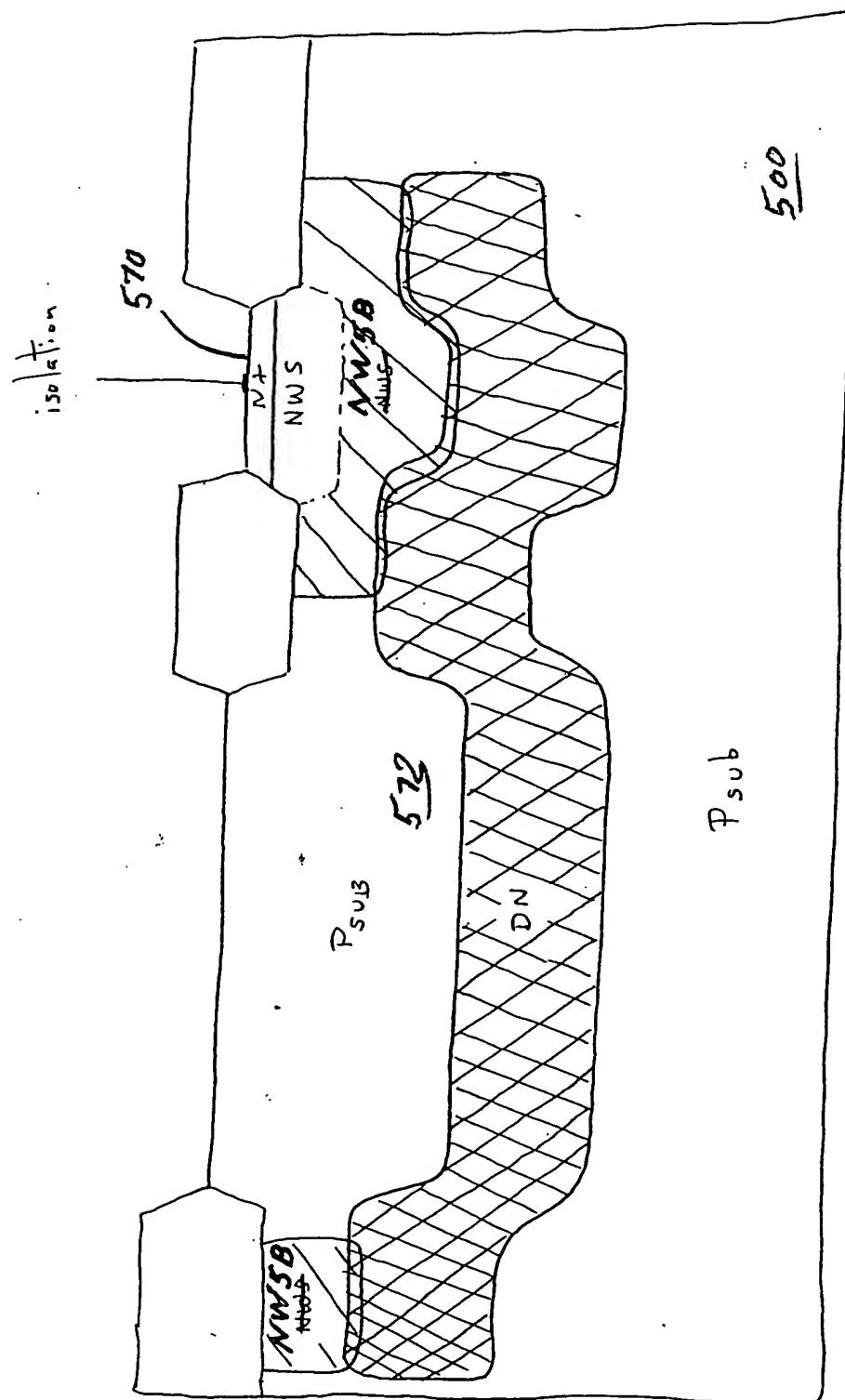


Fig. 14 I.

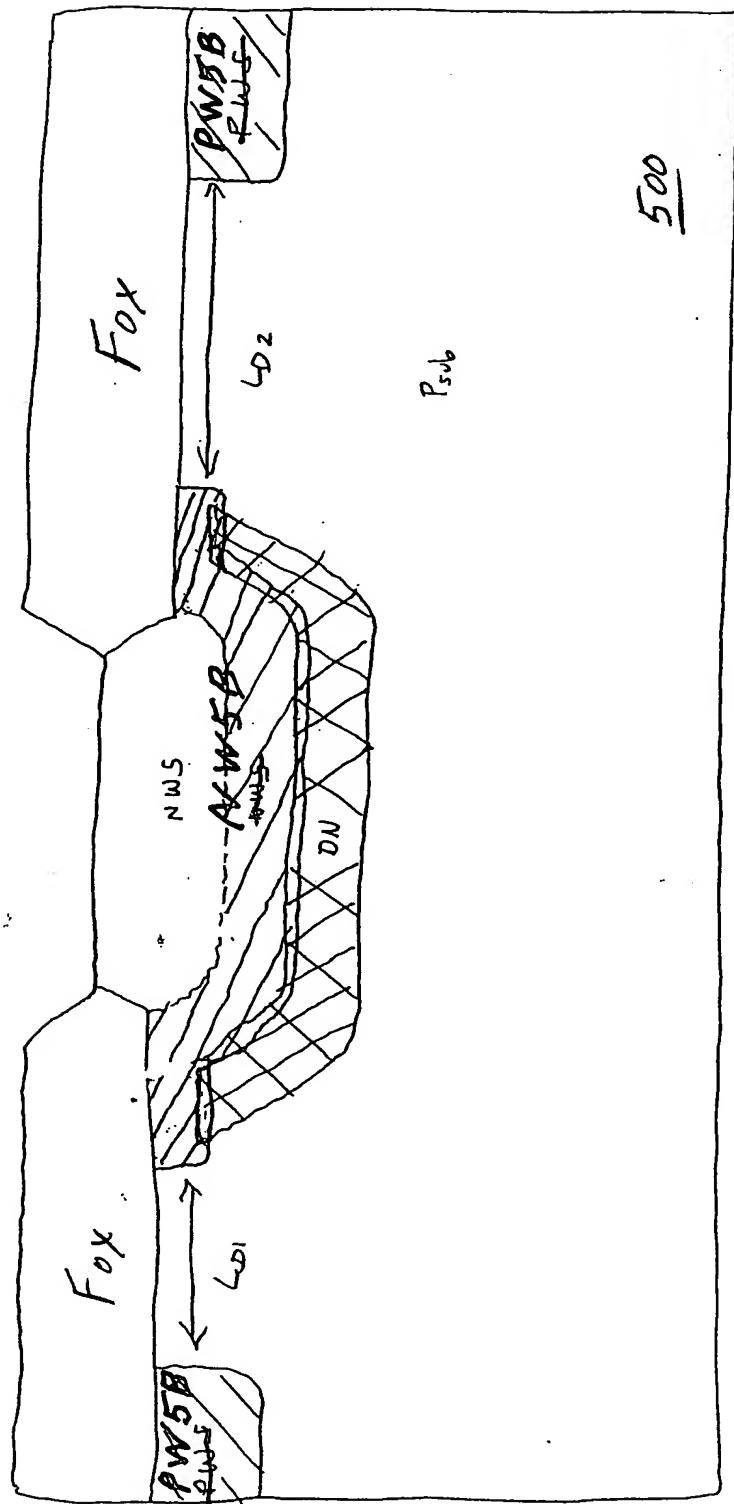


Fig. 14 J

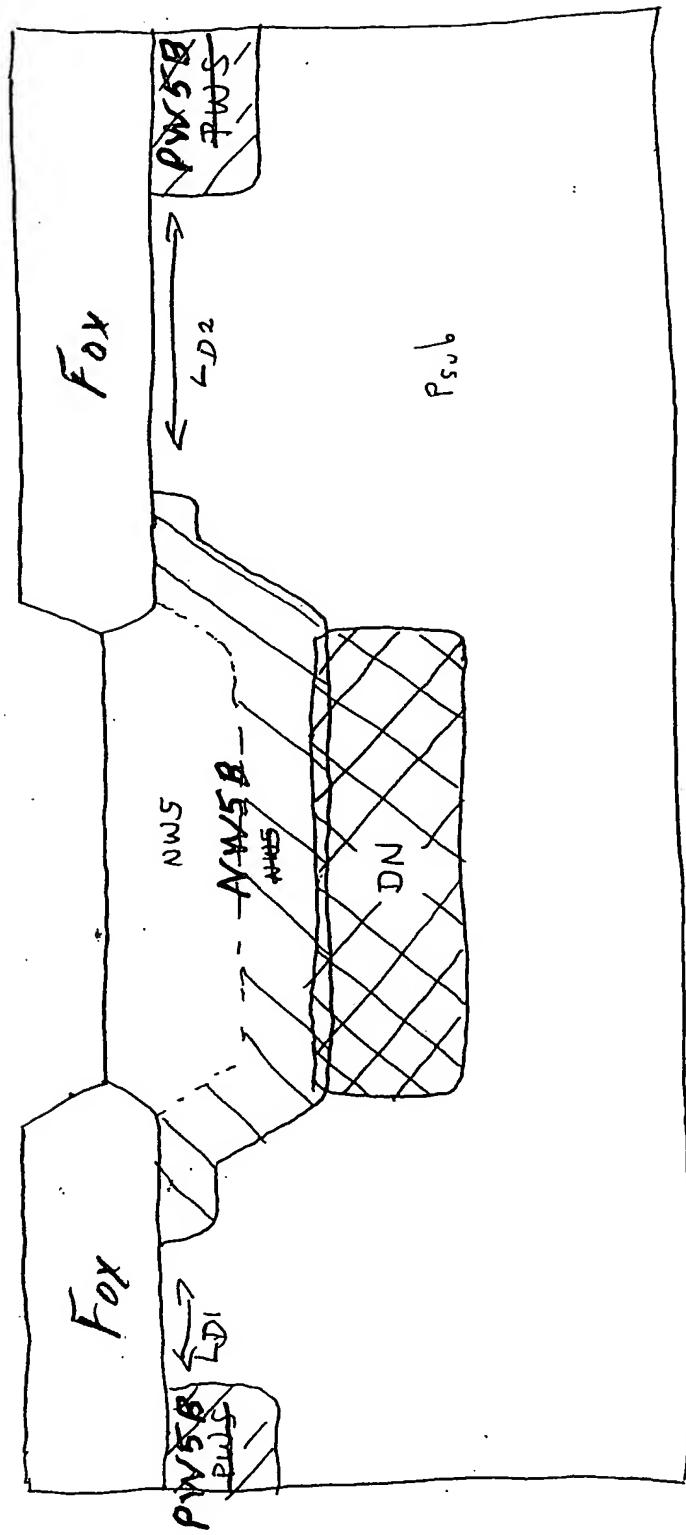


Fig. 14.K

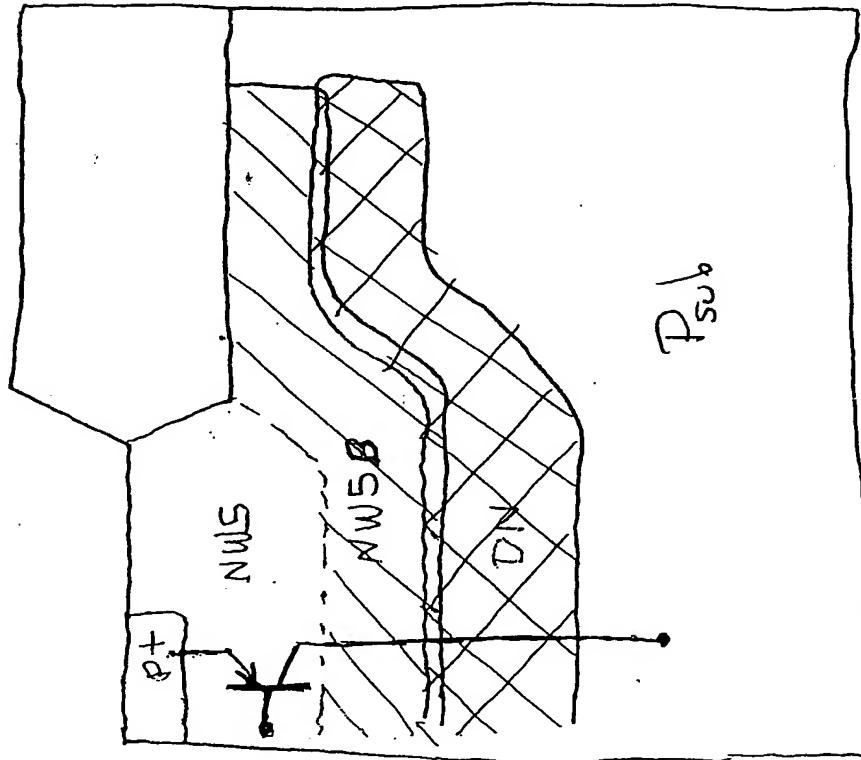
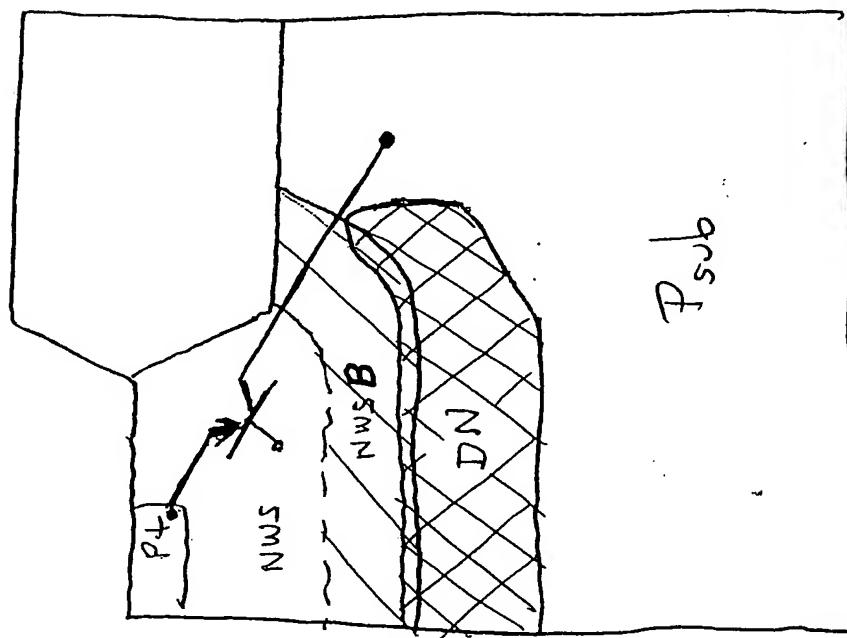


Fig. 14.L

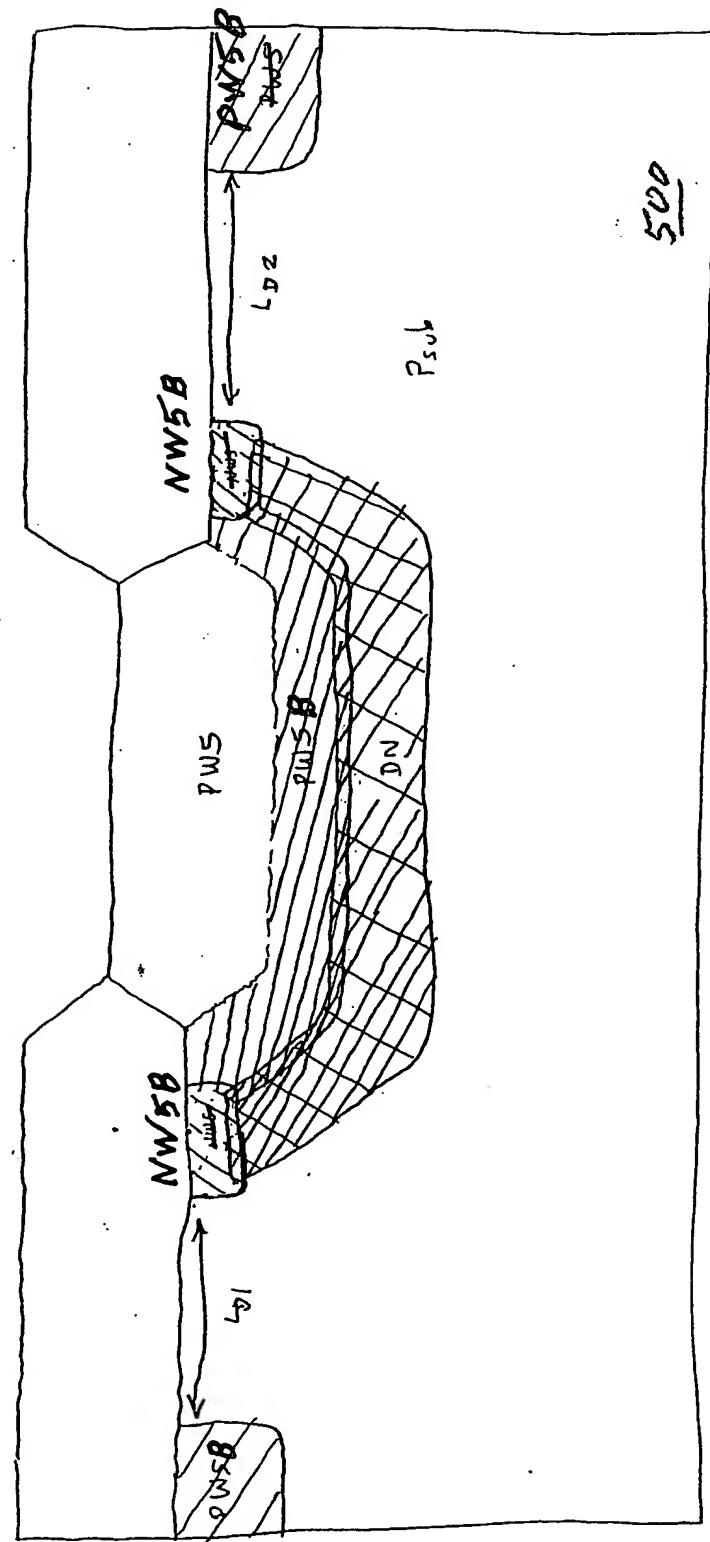


53/219

53/219

53/219

Fig. 14. A



54/219

Fig. 14 P

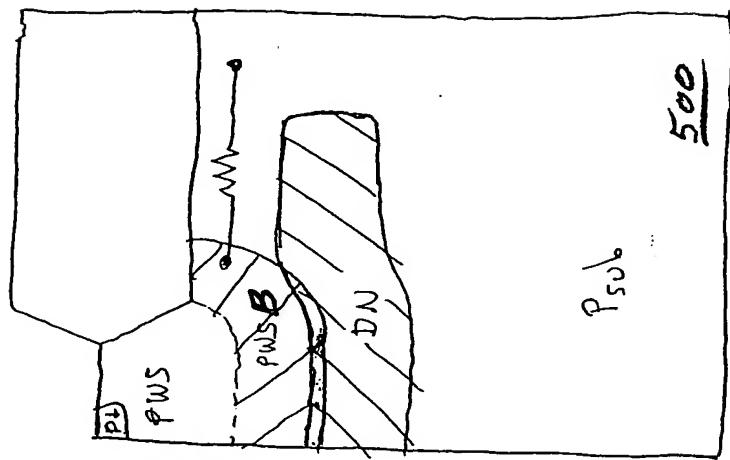


Fig. 14 O

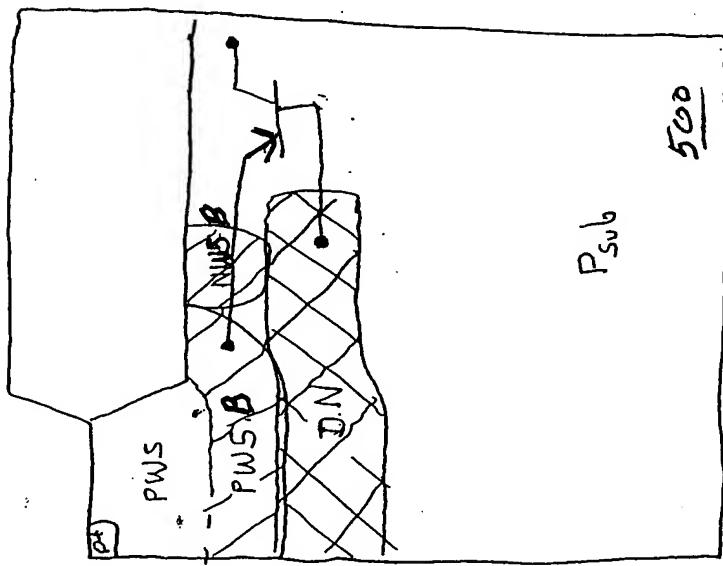


Fig. 14 N

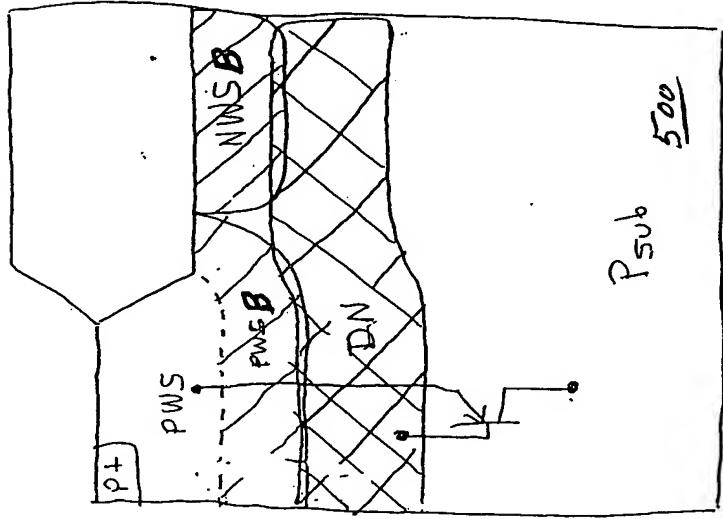
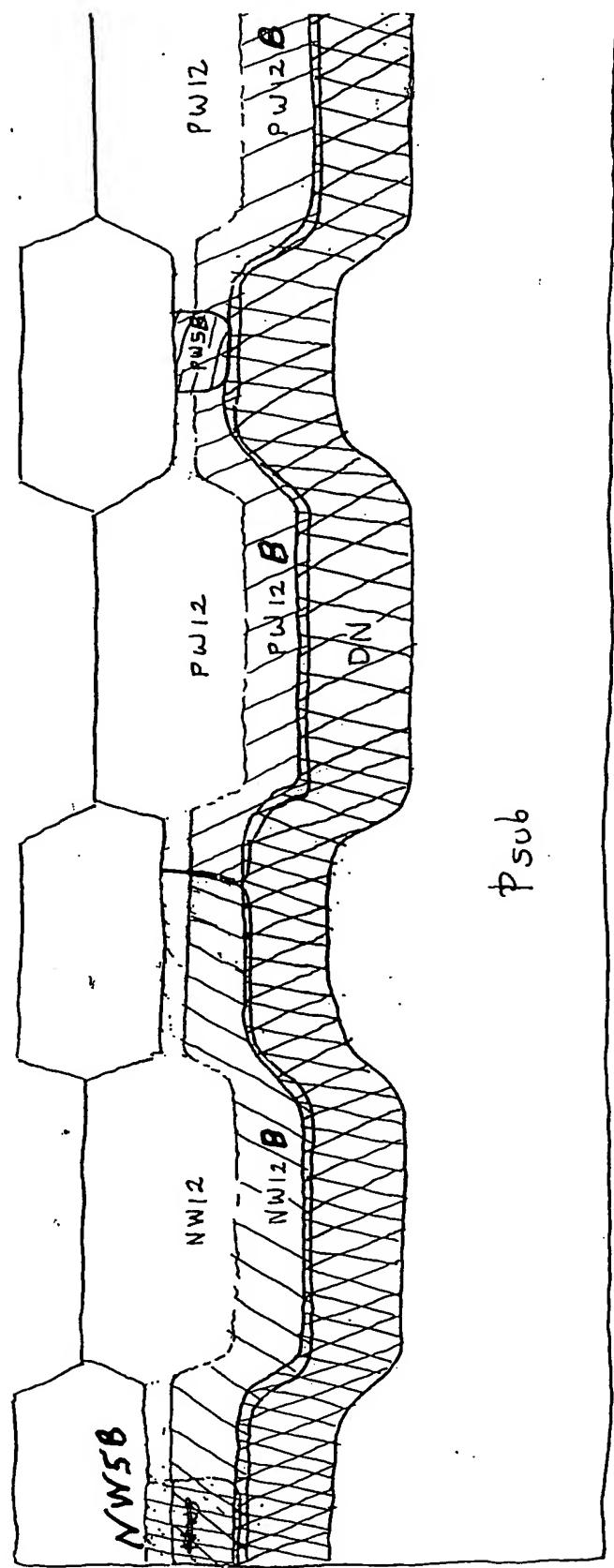


Fig. 15A



10

65 179

60/219

卷之三

Fig. 16A

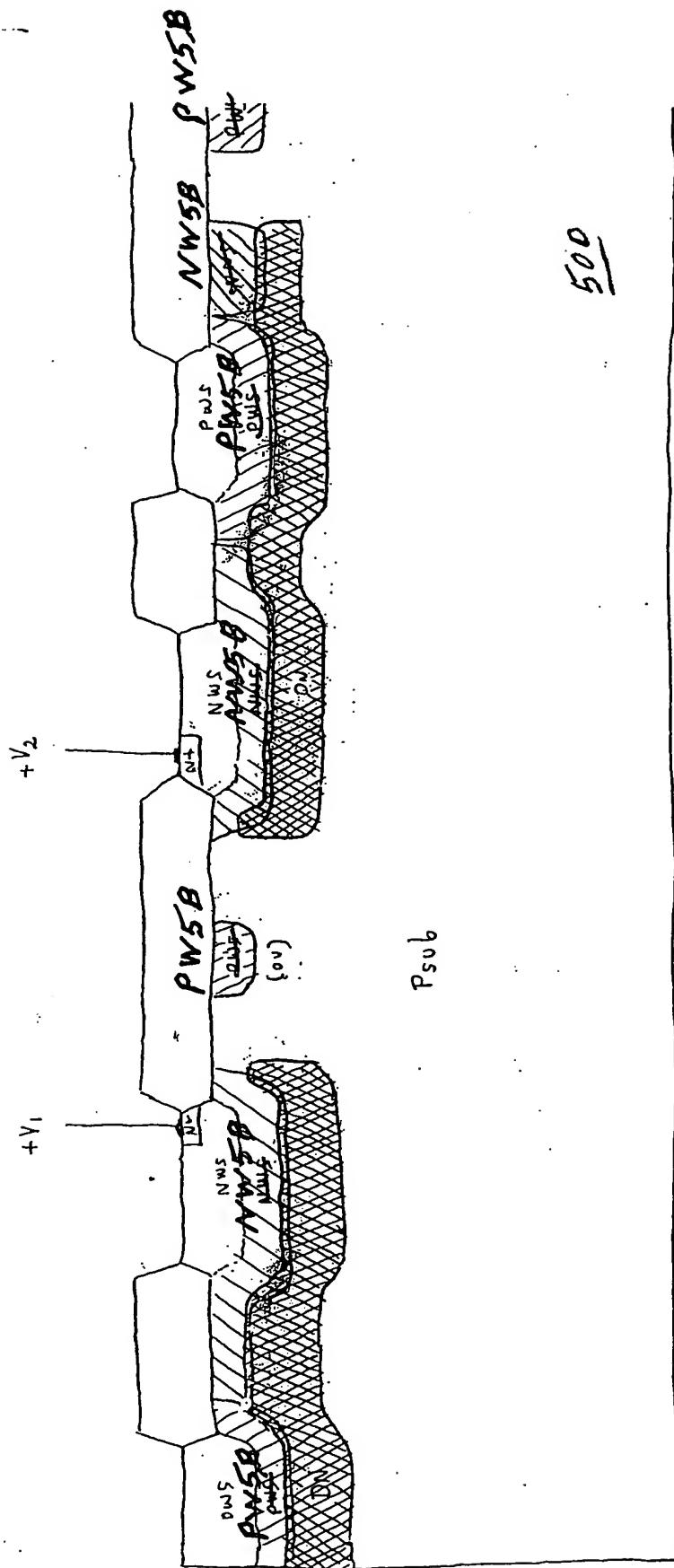
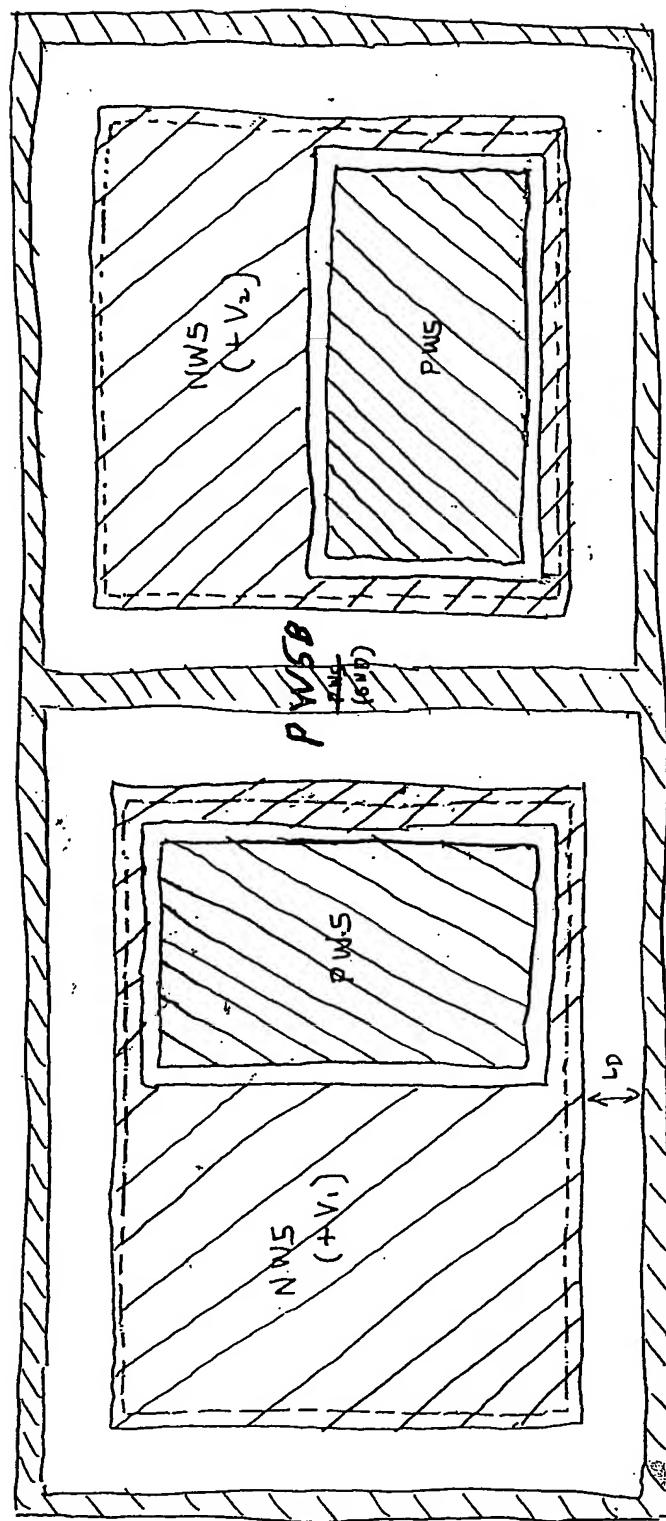
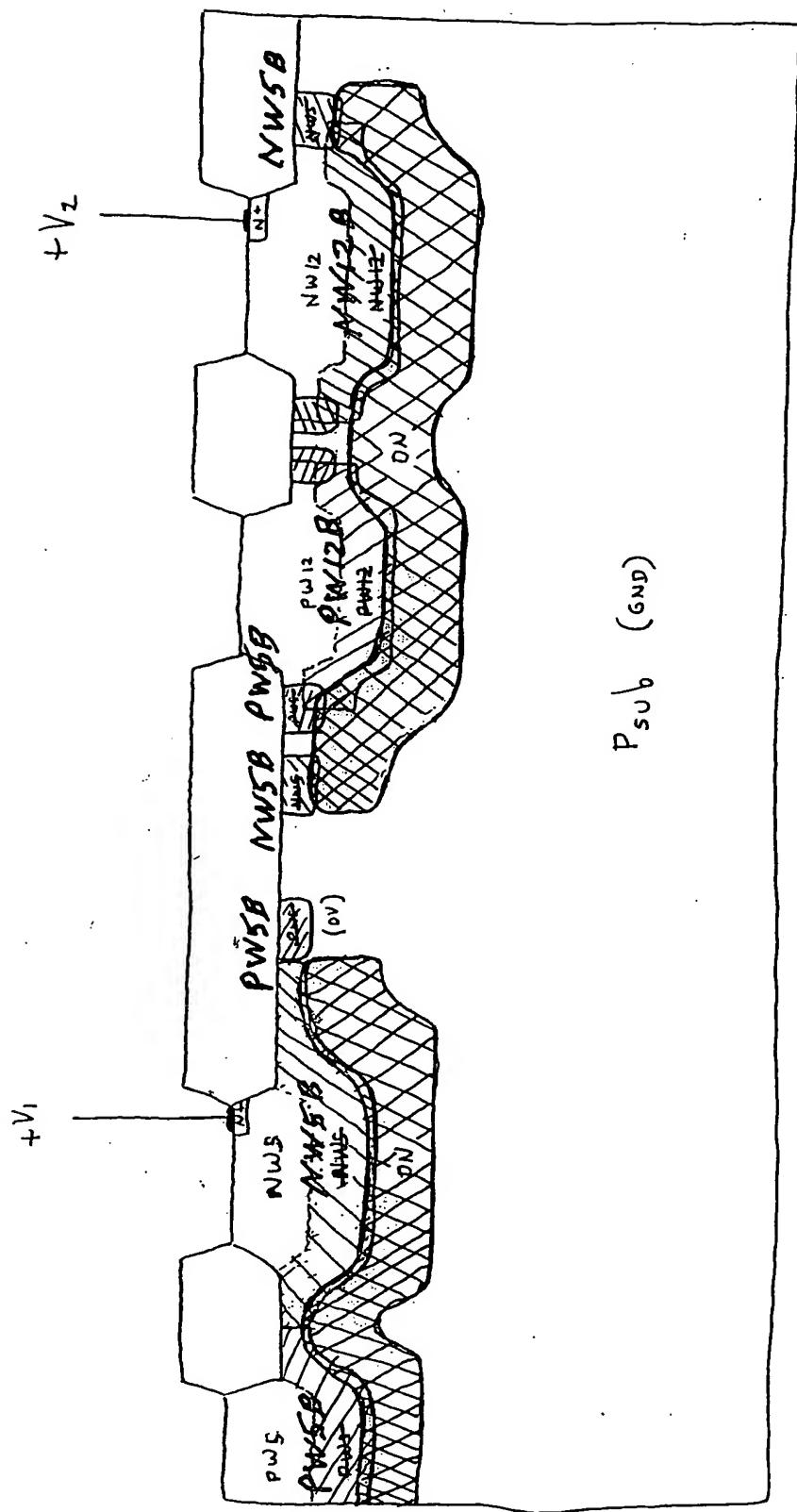


Fig. 16.3



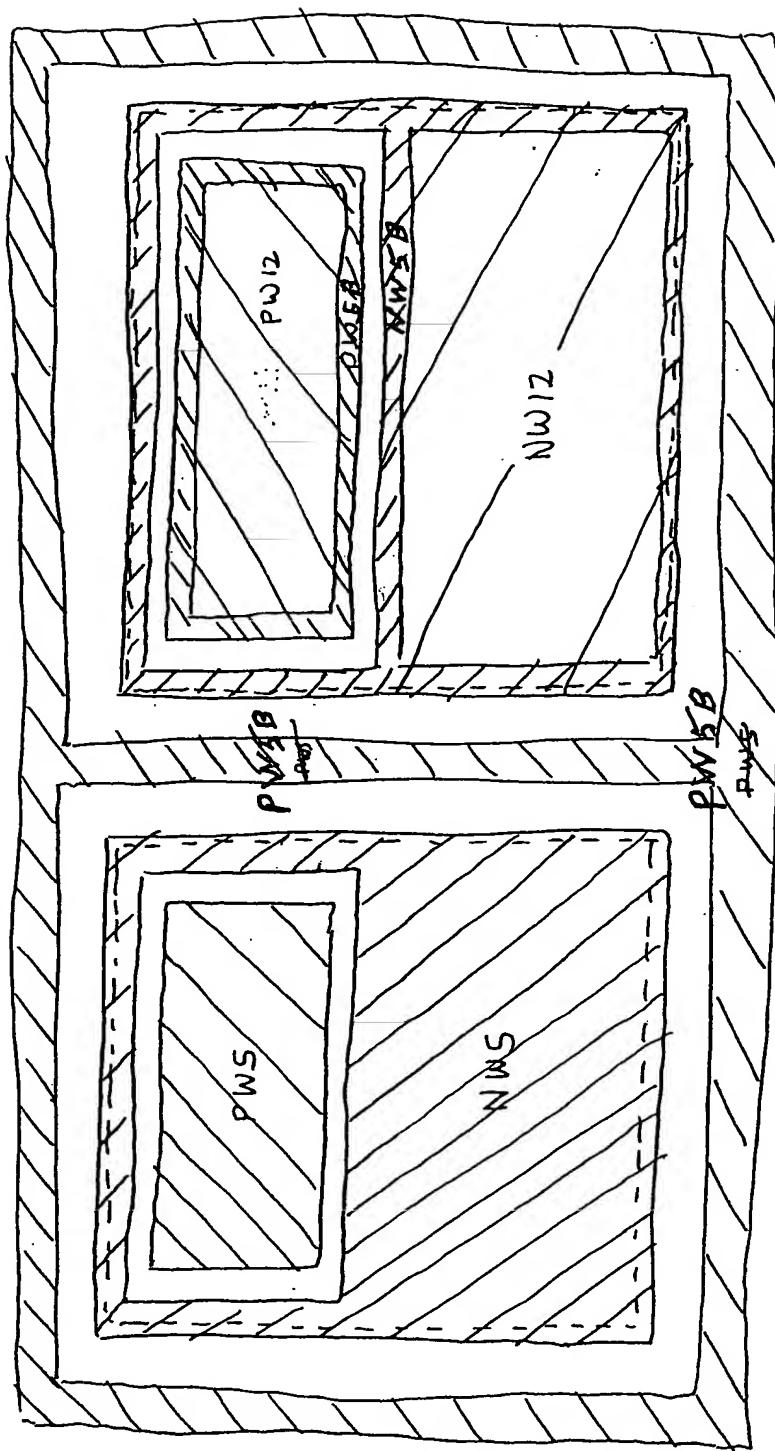
63/219

Fig. 16D



65/219

Fig. 16F



73/219

Fig. 17Q

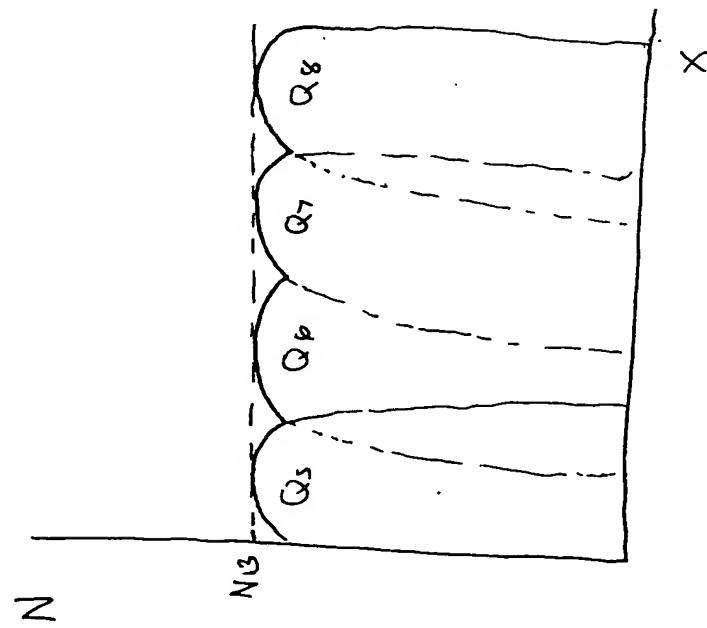
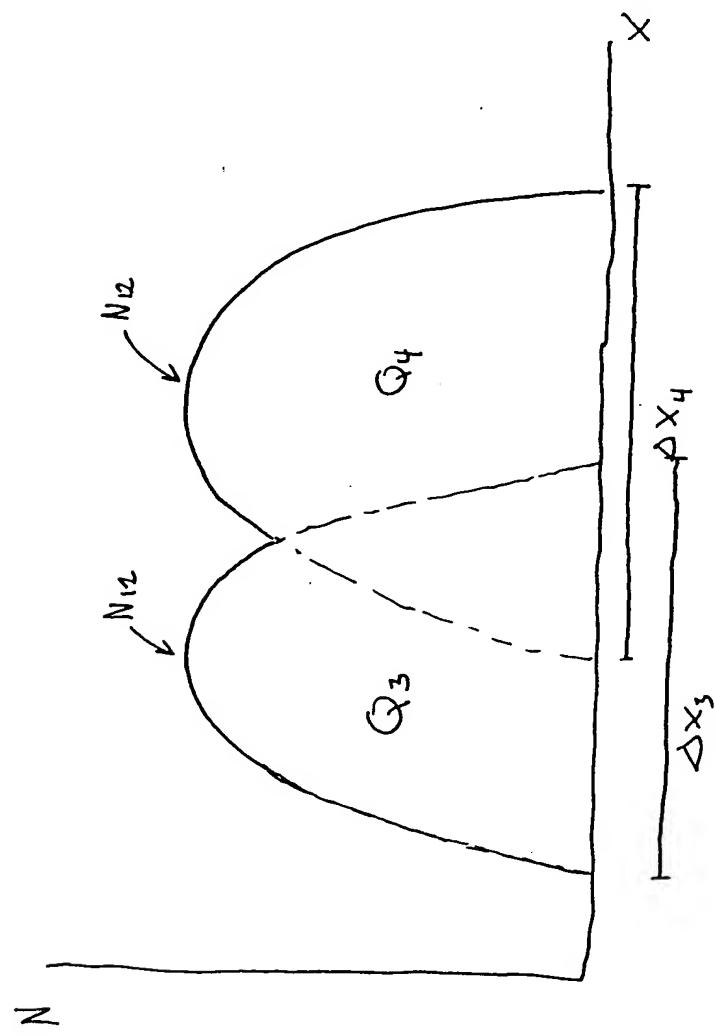


Fig. 17Q



74/219

Fig. 178

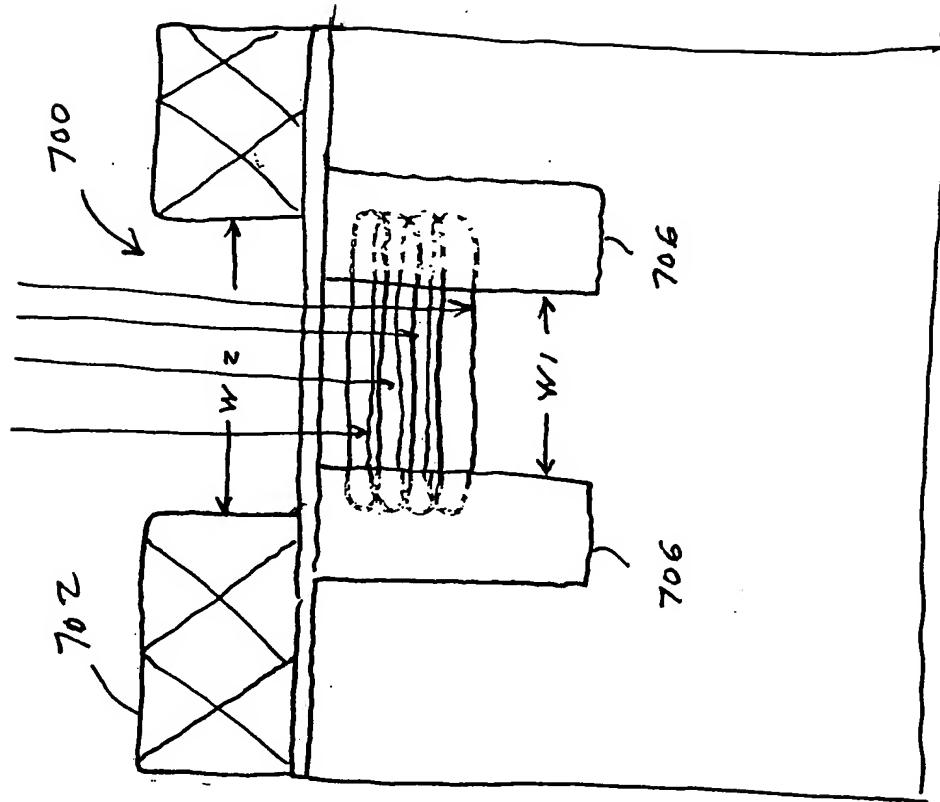
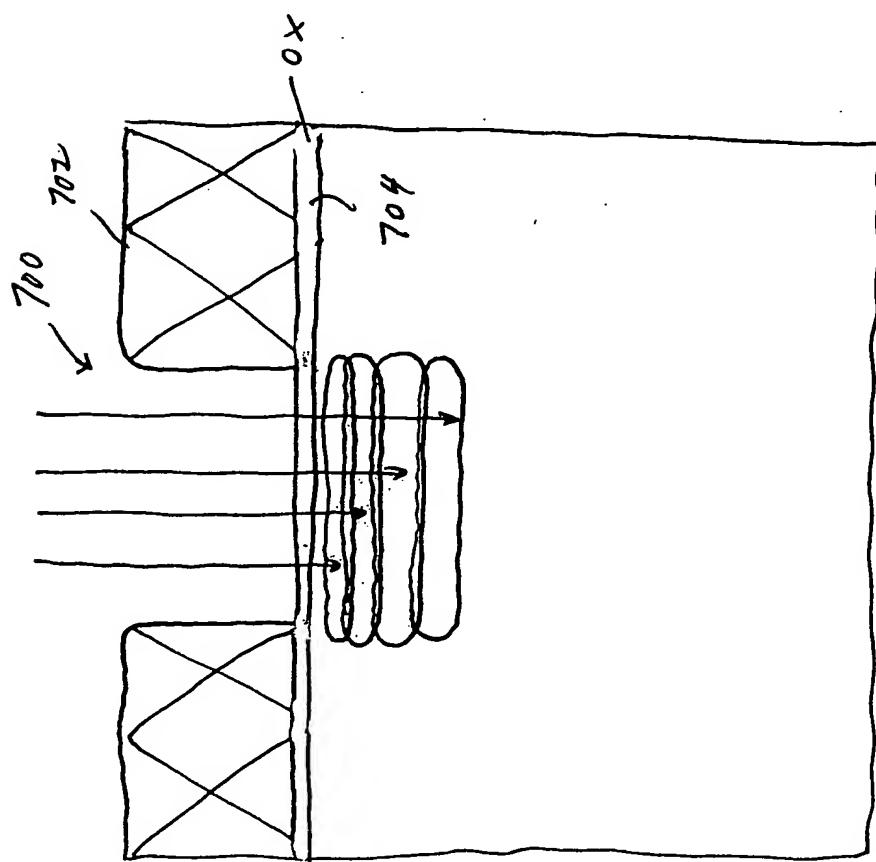


Fig. 179



75/219

Fig. 17A

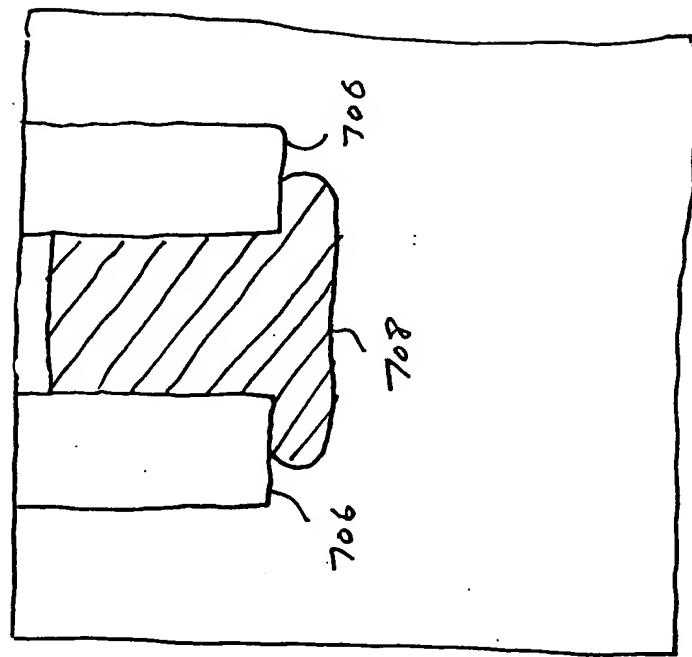
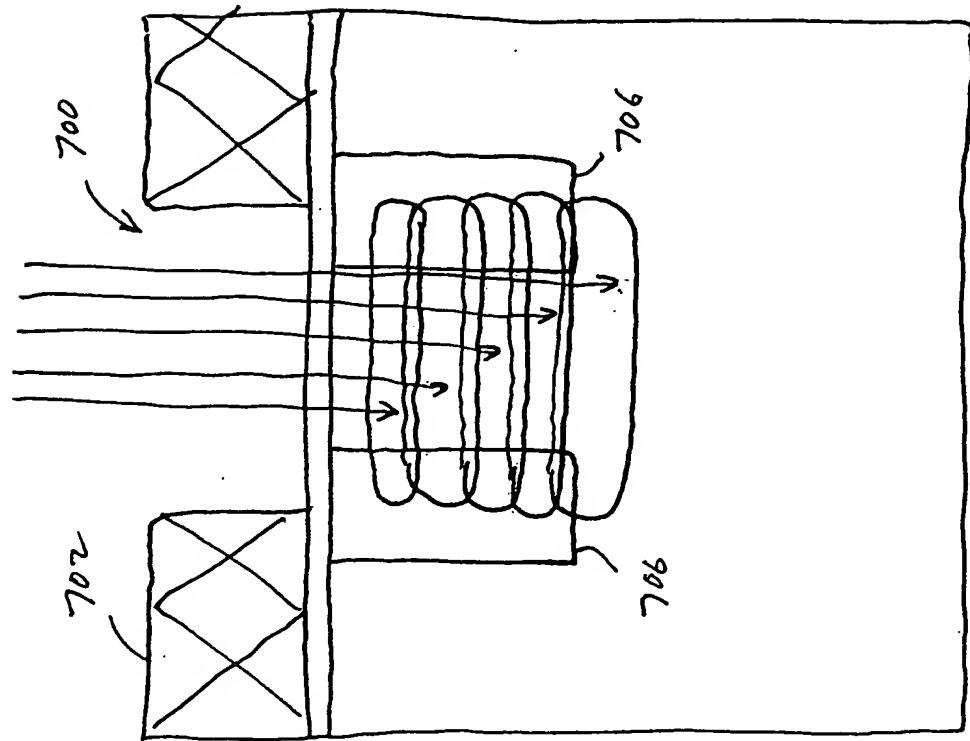


Fig. 17S



77 / 219

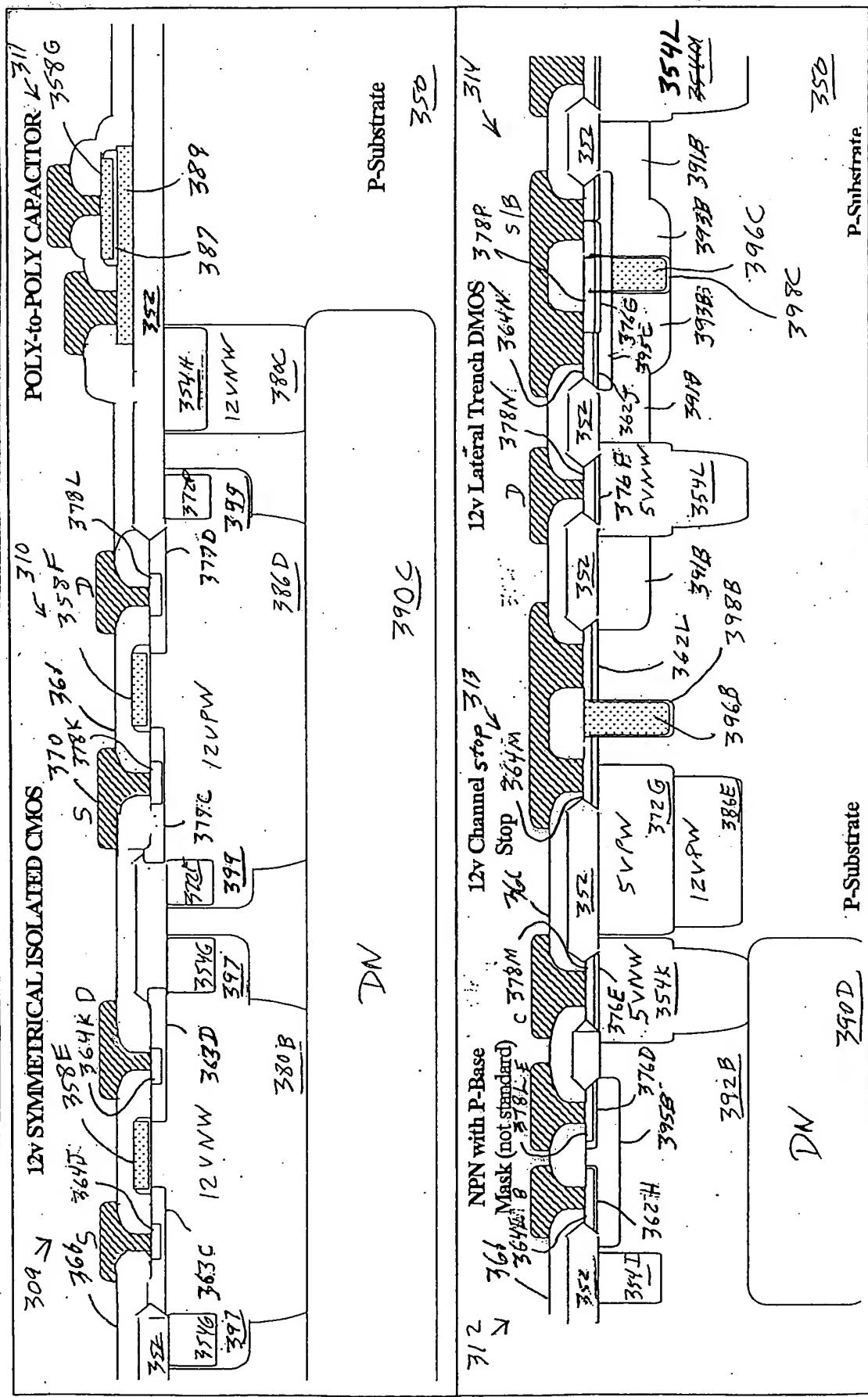


Fig. 18B

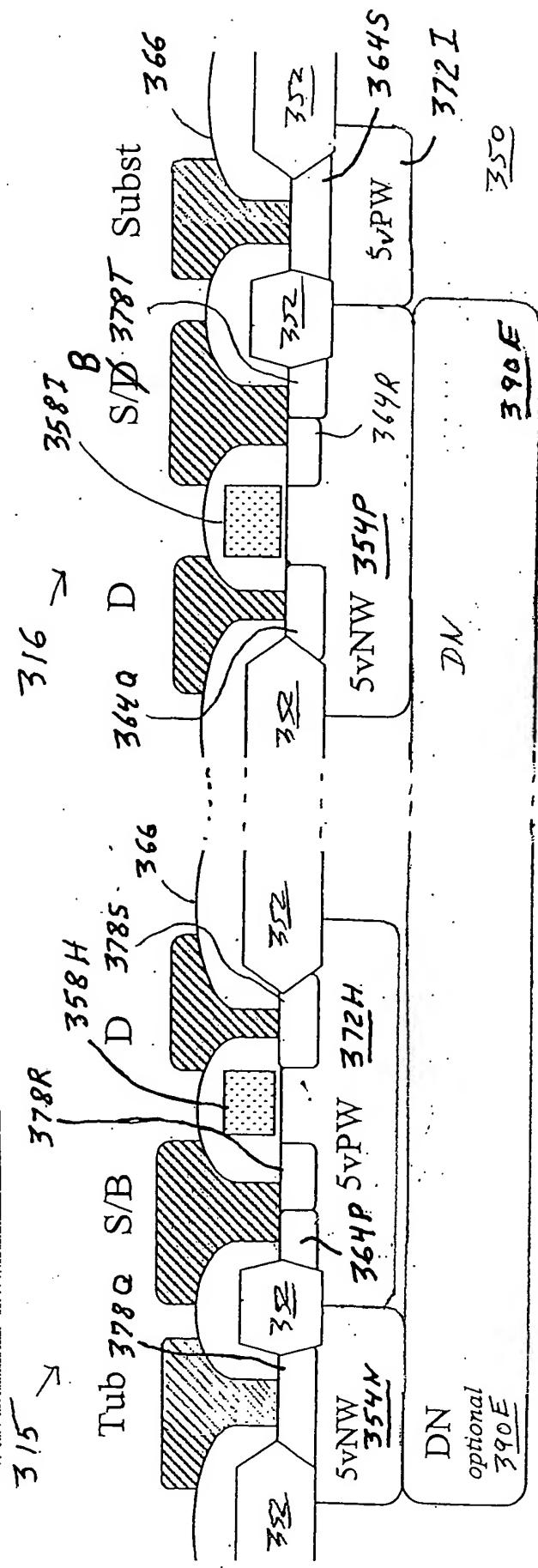
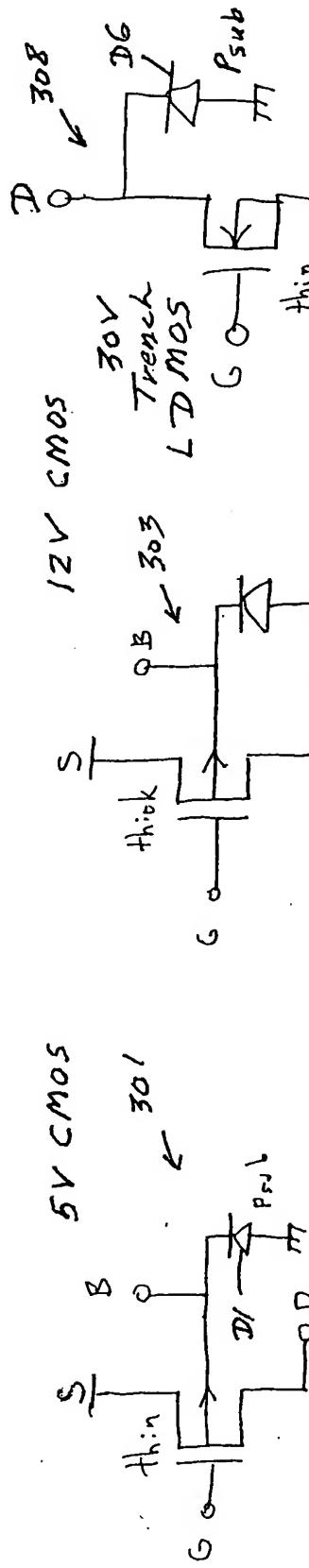


Fig. 18C

83/219



The diagram shows a logic circuit. The inputs are  $G$ ,  $O$ ,  $D$ , and  $B$ . The output  $FI$  is the output of an inverter. The output  $D2$  is the output of an OR gate. The output  $D3$  is the output of a 3-to-8 decoder. The output  $S$  is the output of a 3-to-8 decoder. The input  $G$  is connected to the enable input of the decoder. The inputs  $O$  and  $D$  are connected to the data inputs of the decoder. The input  $B$  is connected to the enable input of the OR gate.

5V NPN

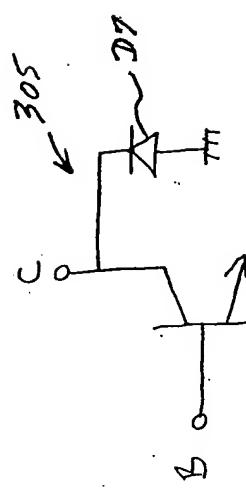


Fig. 19C

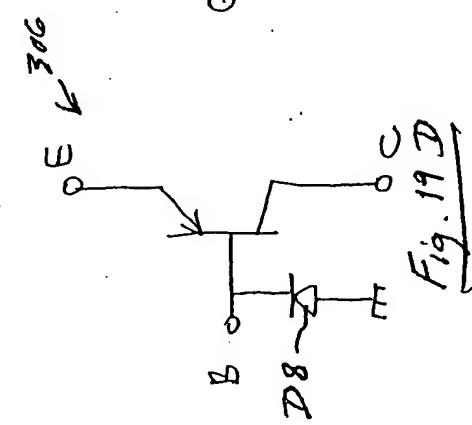


Fig. 19B O S

Diagram of a thin-film resistor circuit (Fig. 19 A). The circuit consists of a thin-film resistor (thin) with a voltage-controlled voltage source (VCSV) and a diode. The circuit includes a 30Ω resistor, a 10Ω resistor, and a 10Ω diode. The output voltage is labeled  $V_{out}$ .

518 8N8

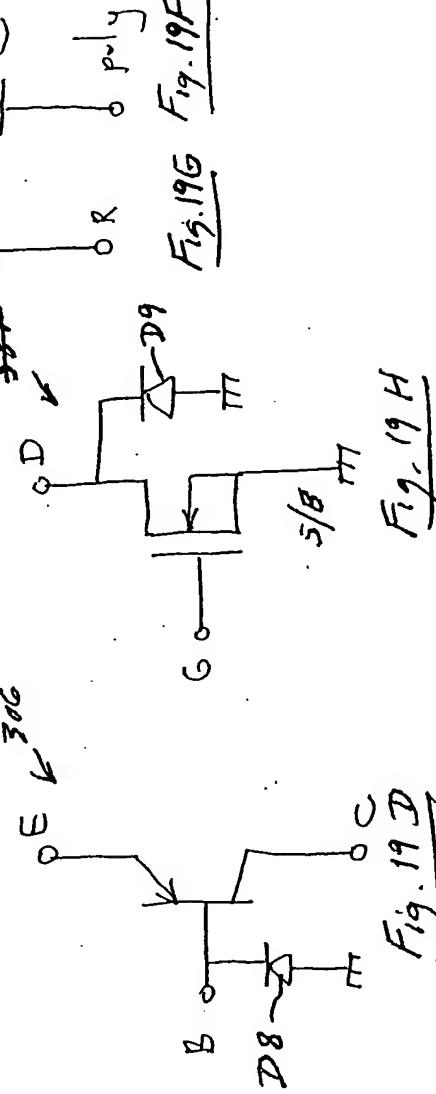


Fig. 19 H

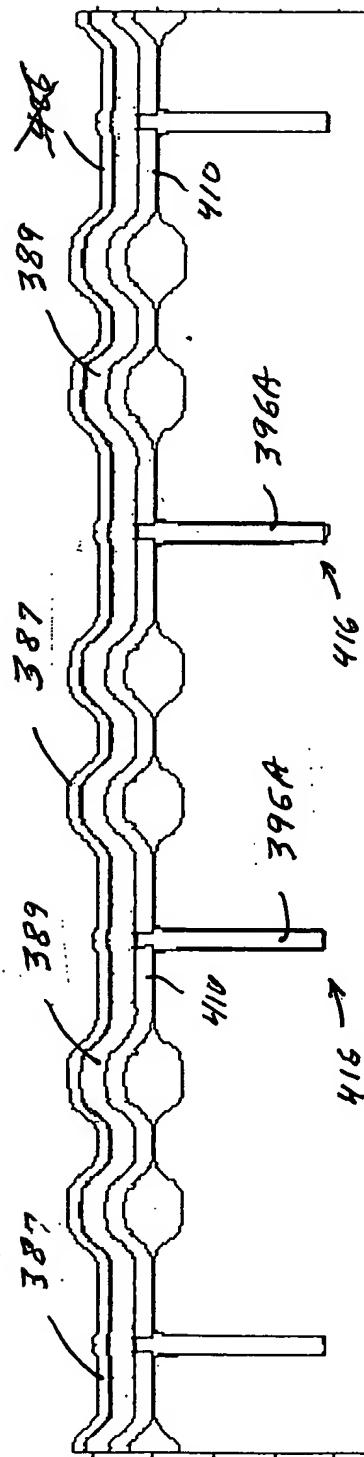
Fig. 19 D

Fig. 19C

The diagram shows a circuit for Fig. 19G. At the top, there is a vertical line with a resistor labeled 'poly' in the middle. Below this is a horizontal line with a capacitor labeled 'C' in the middle. A vertical line labeled 'D9' descends from the bottom of the horizontal line to a diode symbol. The diode is connected to a ground plane. A feedback line labeled 'D' originates from the junction of the diode and the horizontal line, goes up, then down, then up again to connect to the 'poly' resistor. A label '320' is placed above the 'poly' resistor, and a label '382' is placed below it. The entire circuit is labeled 'DR LDMOS' at the bottom left.

110/219

30V Lateral Trench DMOS 308

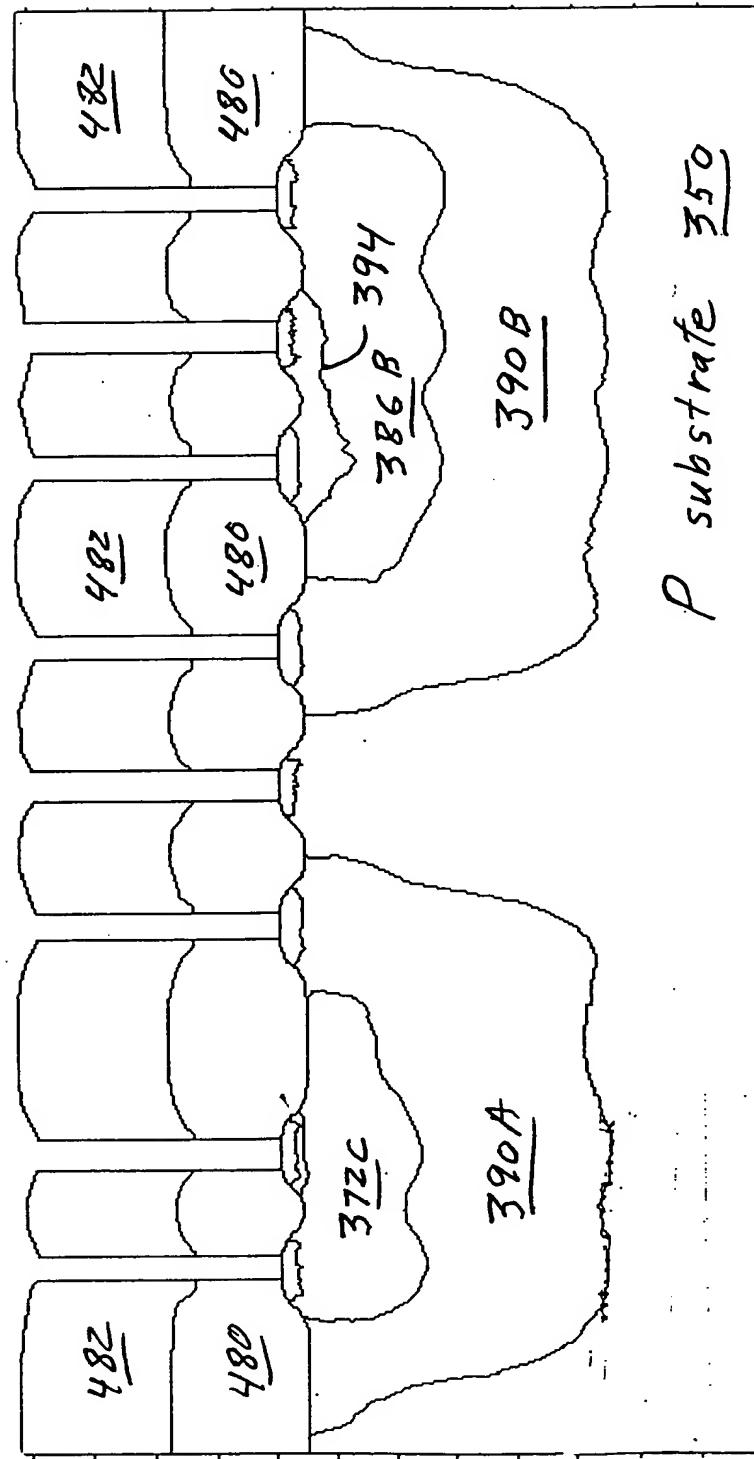


$P_{\text{substrate}}$  350

Interlayer Dielectric  
Fig 33D

196/219

High  $F_T$  Layout  
 $5V NPN 305$   
 $5V PNP 306$



Interlayer Dielectric Deposition and Etch

Fig. 64B

215/219

Fig. 17X <sup>U</sup>

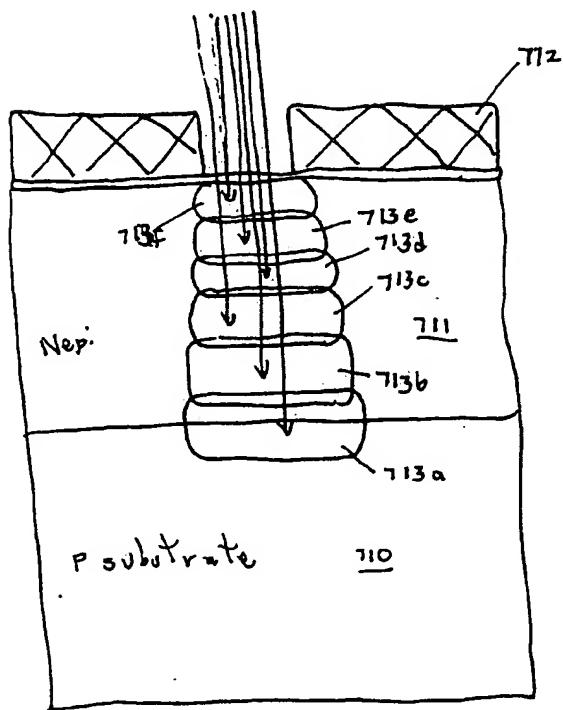


Fig. 17X <sup>V</sup>

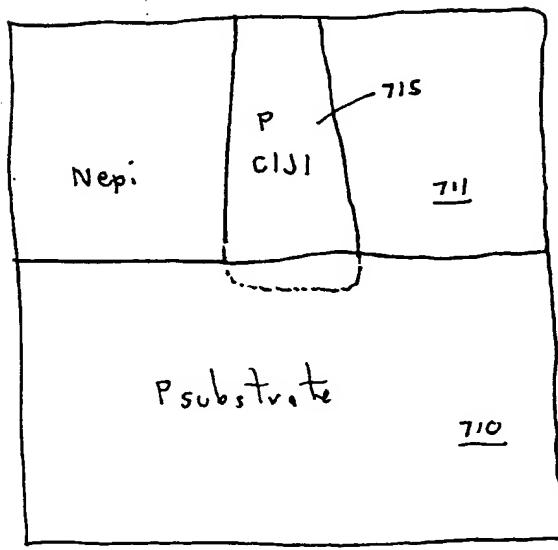


Fig. 17X

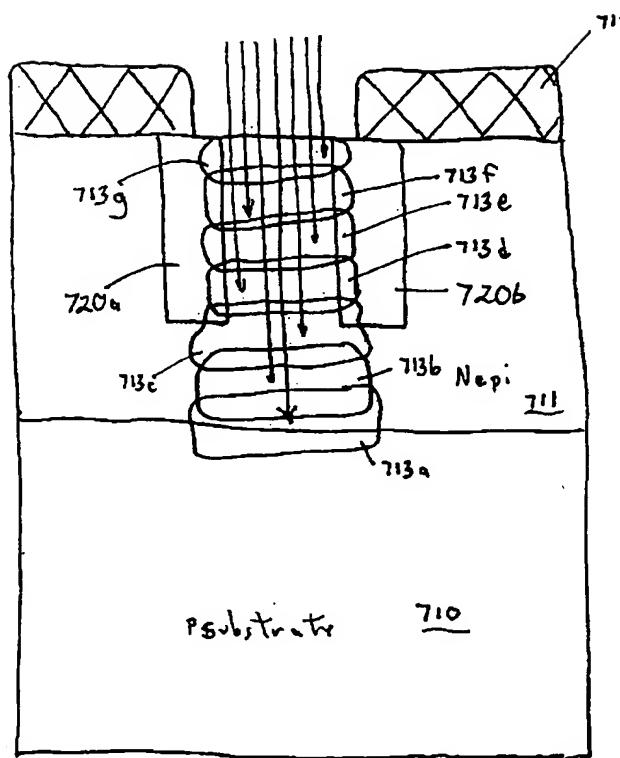
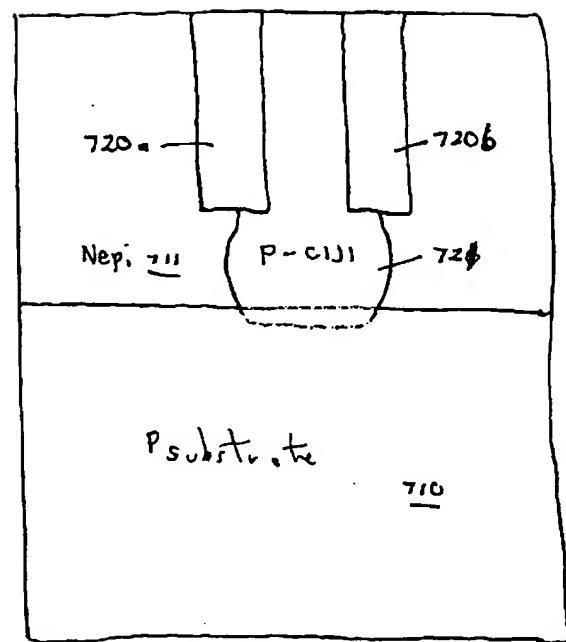


Fig. 17Y



217/219

Fig. 17F

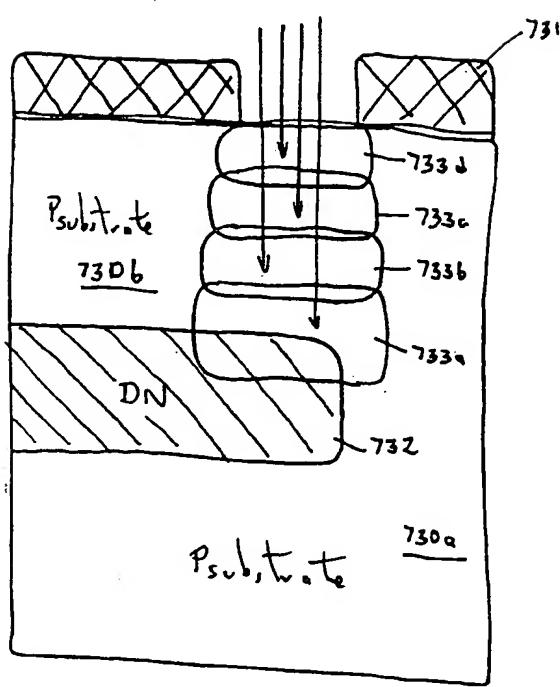
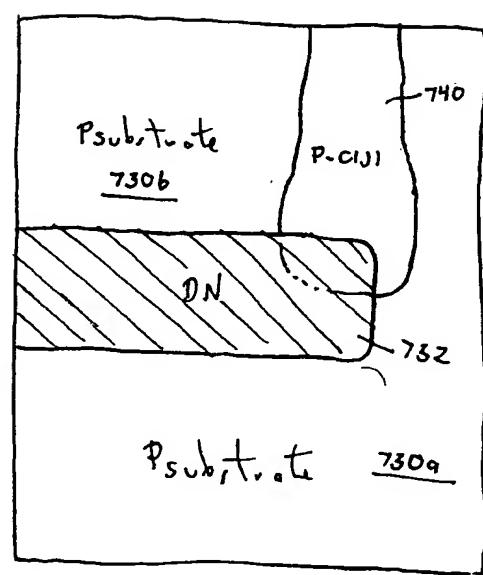


Fig. 17AA



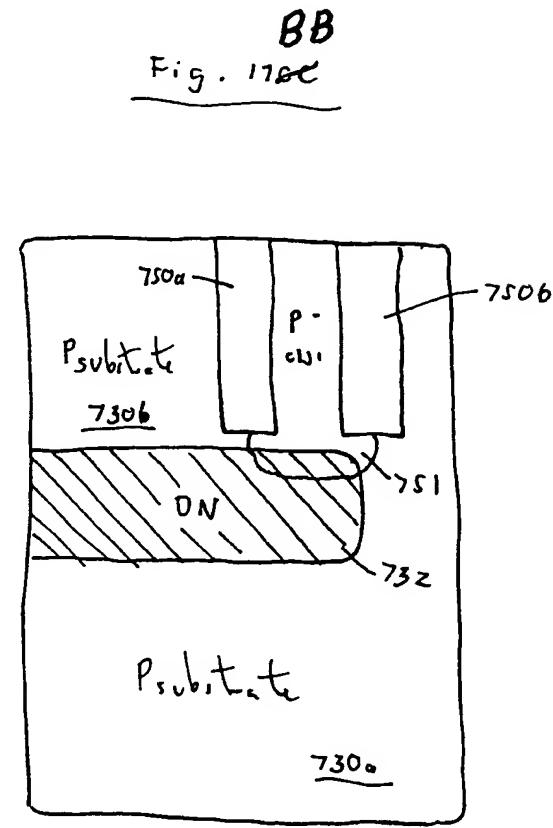
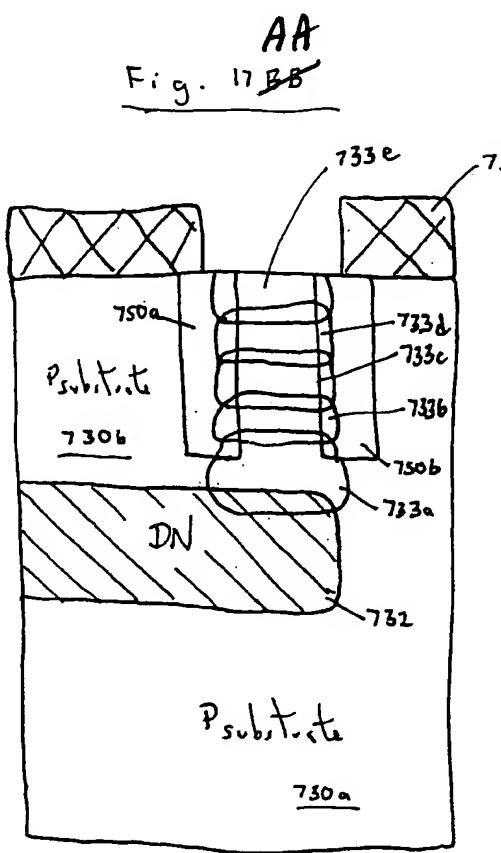
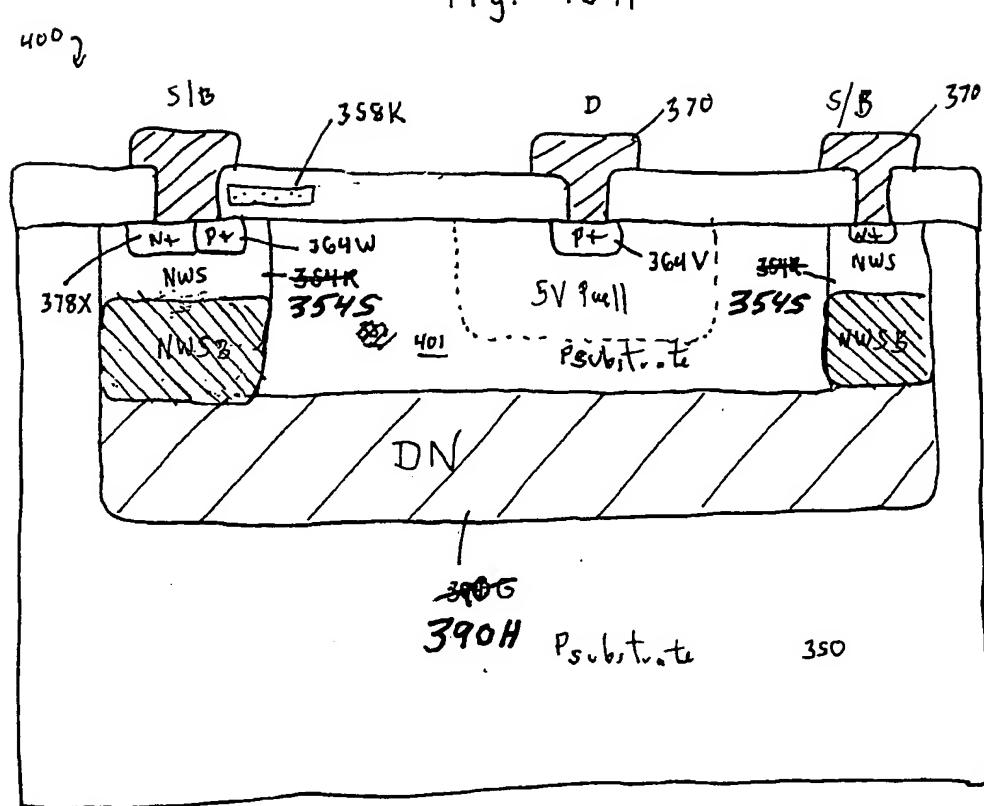


Fig. 18 H



**This Page is Inserted by IFW Indexing and Scanning  
Operations and is not part of the Official Record**

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images include but are not limited to the items checked:

- BLACK BORDERS**
- IMAGE CUT OFF AT TOP, BOTTOM OR SIDES**
- FADED TEXT OR DRAWING**
- BLURRED OR ILLEGIBLE TEXT OR DRAWING**
- SKEWED/SLANTED IMAGES**
- COLOR OR BLACK AND WHITE PHOTOGRAPHS**
- GRAY SCALE DOCUMENTS**
- LINES OR MARKS ON ORIGINAL DOCUMENT**
- REFERENCE(S) OR EXHIBIT(S) SUBMITTED ARE POOR QUALITY**
- OTHER:** \_\_\_\_\_

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning these documents will not correct the image problems checked, please do not report these problems to the IFW Image Problem Mailbox.**